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Fixed Width Booth Multiplier using Error Compensation

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Abstract— In many multimedia and digital-signal processing (DSP) applications, multipliers are considered to be the basic arithmetic units. These multipliers significantly influence the system's performance and power dissipation. To achieve high performance, the modified Booth encoding has been widely adopted in parallel multipliers. It reduces the number of partial products through performing multiplier re-coding. The number of adder cells in the Booth multiplier architecture can be reduced by various techniques. The process of truncation can be done so that the multiplier structure can be simplified to form a fixed width multiplier. The *2n* bit product that is to be obtained from the multiplication of *n* bit multiplicand and *n* bit multiplier is truncated to *n* output bits by eliminating the adder cells needed for the addition of *n* least-significant bits (LSBs). The elimination of certain adder cells can cause truncation error. Hence, appropriate compensation biases are to be introduced into the retained adder cells. The compensation circuit needed for reducing truncation error is also designed here. Our proposed encoder was simulated in Mentor Graphics Model Sim 10.1c, using Verilog HDL. The output of the encoder was synthesized using Leonardo Spectrum. The synthesis results show that the critical path delay as well as the total number of gates is reduced when compared with the prevailing technology.

Index Terms— Booth multiplication, Radix-4, modified Booth multiplication, carry save adder, carry look ahead adder, Booth encoder, partial product matrix.

1 Introduction

Low power dissipation, area minimization and improved processing performance are the major factors of concern in many multimedia and digital signal processing (DSP) systems. Multipliers can be considered to be the fundamental arithmetic unit in these systems and they can influence the system performance and power dissipation significantly. To achieve high performance, the modified Booth encoding which reduces the number of partial products through performing the multiplier recoding has been widely adopted in multipliers [1]-[3]. Moreover, $n \times n$ fixed-width multipliers that generate only the n most significant product bits are frequently utilized to maintain a fixed word size such that significant hardware complexity reduction and power saving can be achieved. This is made possible by directly removing the adder cells of standard multiplier for the computation of the n least significant bits of $2n$-bit output product. However, a huge truncation error will be introduced to this kind of direct-truncated fixed-width multiplier (DTFM).

To effectively reduce the truncation error, various error compensation methods, which add estimated compensation value to the carry inputs of the reserved adder cells, have been proposed. The error compensation value can be produced by the constant scheme or the adaptive scheme. The constant scheme [4], [5] pre-computes the constant error compensation value and then feeds them to the carry inputs of the retained adder cells when performing multiplication operations regardless of the influence of the current input data value. With the advantage of simplification, the truncation error of the constant scheme is relatively large. On the contrary, the adaptive scheme [6]-[8] was developed to achieve higher accuracy than the constant scheme through adaptively adjusting the compensation value according to the input data at the expense of a little higher hardware complexity. However, most of the adaptive error compensation approaches are developed only for fixed-width array multipliers and cannot be applied to significantly reduce the truncation error of fixed-width modified Booth multipliers directly. To overcome this problem, several error compensation approaches [9]-[11] have been proposed to effectively reduce the truncation error of fixed-width modified Booth multipliers. In certain approaches, the compensation value was generated by using statistical analysis and exhaustive simulation analysis.

In this project work, an error compensation circuit for the fixed-width modified Booth multiplier with higher accuracy and simpler hardware structure is proposed. To obtain better performance with a simple error compensation circuit, Booth encoded outputs are utilized to generate the error compensation value. To accomplish this goal, a simple compensation circuit composed of simple logic gates is developed according to the proposed error compensation function. Simulation and implementation results show that the proposed fixed-width modified Booth multiplier actually achieves much higher performance than existing fixed-width modified Booth multipliers [12].

This paper is organized as follows. In section II the modified Booth multiplier fundamentals are reviewed. Section III deals with the proposed Booth encoder circuit. Section IV deals with the results obtained from the simulation and synthesis. Finally, section V concludes the paper.

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2 Fundamental Of Modified Booth Multiplier

Signed multiplication is a careful process. With unsigned multiplication, there is no need to take the sign of the number into consideration. However in signed multiplication, the same process cannot be applied because the signed number is in a 2's complement form which would yield an incorrect result if multiplied in a similar fashion to unsigned multiplication. In this case Booth's algorithm [13] can be used since it preserves the sign of the result. Booth multiplication can be even more efficiently done by reducing the number of partial product rows. This is made possible by radix 4 or radix 8 modified Booth multiplication techniques.

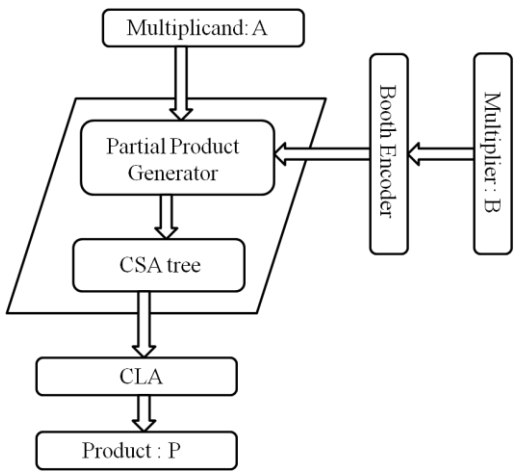

Fig.1. Block diagram of modified Booth multiplication.

The basic structure of a modified Booth multiplier is given in figure 1. It has hardware structures for Booth encoder, partial product generator, the Carry save adder tree and the final Carry lookahead adder. The multiplier is recoded and encoded using the Booth encoder. Based on the Booth encoder output, the partial products are generated. The partial product rows are then added using the Carry save tree and the carry lookahead adder does the final addition.

The multiplication operation of two n bit signed numbers $A = a_{n-1}a_{n-2}\ldots a_0$ (multiplicand) and $B = b_{n-1}b_{n-2}\ldots b_0$ (multiplier) shall be considered. The numbers can be expressed in their two's complement as:

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i, \qquad B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \qquad (1)$$

Multiplier recoding [10] is the process by which the multiplier is recoded such that reductions in the number of partial product rows are made possible depending on the recoded multiplier.

For modified Booth encoding, a "0" must always be concatenated to the right of B, and n should be even. By modified Booth encoding [12] which groups the bits of the multiplier into triplets, B can be expressed as

$$B = \sum_{i=0}^{\frac{n}{2}-1} (-2b_{2i+1} + b_{2i} + b_{2i-1}) 2^{2i} \qquad (2)$$

Table I. summarizes the coding operation by equation (2).

Table I. Modified Booth encoding table.

b_{2i+1}	b_{2i}	b_{2i-1}	b'_i	Neg_i	Two_i	One_i	$Zero_i$	Cor_i
0	0	0	0	0	0	0	1	0
0	0	1	+A	0	0	1	0	0
0	1	0	+A	0	0	1	0	0
0	1	1	+2A	0	1	0	0	0
1	0	0	-2A	1	1	0	0	1
1	0	1	-A	1	0	1	0	1
1	1	0	-A	1	0	1	0	1
1	1	1	0	1	0	0	1	0

Figure 2. shows Grouping of multiplier bits for n = 8. It demonstrates how multiplier recoding is done. Here the operation to be performed is determined by b'_i. The Booth encoder is designed based on the truth table given in table I. The input bits are the triplets which are taken as inputs for multiplier recoding. The operations to be performed are determined by the Booth encoder. The encoder outputs are used to choose one of multiple multiplicands -2A, -A, 0, A or 2A for generating each partial product row PP_i.

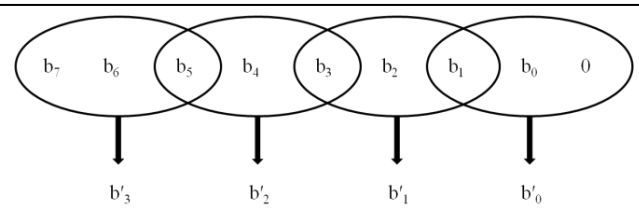

Fig.2. Grouping of multiplier bits for n = 8.

Many real life applications related with digital signal processing systems use fixed width multipliers. In fixed width modified Booth multipliers, the n most significant output bits of the multiplier are kept and the least significant output bits are truncated hence making a multiplier giving n output bits for an $n \times n$ multiplication. The previous works related to fixed width modified Booth multiplier includes multiplier designs using approximate carry generation by exhaustive simulation, approximate carry generation by statistical analysis, compensation circuits using constant scheme or the adaptive scheme etc. The recent work related with fixed width modified Booth multiplier uses a comparison based sorting network for compensation. In this paper, an error compensation circuit for the fixed-width modified Booth multiplier with higher accuracy and simpler hardware structure using simple logic gate is proposed. To obtain better performance with a simple error compensation circuit, Booth encoded outputs are utilized here to generate the error compensation value.

3 Proposed Fixed Width Booth Multiplier

The block diagram of the partial product matrix for modified Booth multiplication is shown in figure 3. Partial products for modified Booth multiplier can be divided into MP and LP as shown in figure.

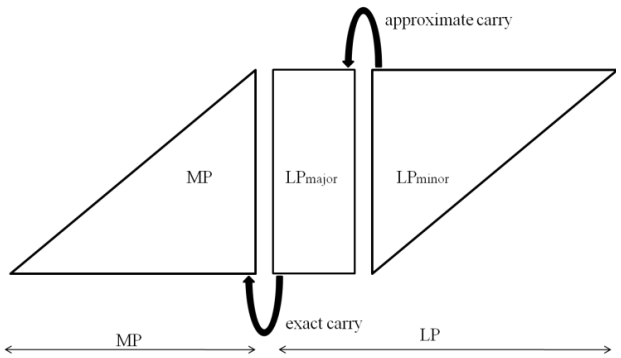

Fig. 3. Block diagram of partial product matrix.

The 2n-bit output product P can be expressed as,

$$P = S\_MP + S\_LP \quad (3)$$

To generate error compensation bias more efficiently, LP can be further divided into LP_{major} and LP_{minor}. From figure 3, notice that LP_{major} has a dominant effect on the carry signals generated from LP part since LP_{major} has the largest weight in the LP part. Also, the generated partial products are directly dependent on the Booth encoder outputs. From figure 3, S_LP can be expressed as,

$$S\_LP = S\_LP_{major} + S\_LP_{minor} \quad (4)$$

3.1 Proposed Booth Encoder and PP generator

The outputs of the proposed Booth encoder can be designed using the Karnaugh map method, where the output bits are realized from the truth table given in table II. The truth table for the proposed Booth encoder is shown in table II.

Table II. Truth table for the proposed Booth encoder.

b_{2i+1}	b_{2i}	b_{2i-1}	b'_i	Neg_i	Two_i	One_i	$Zero_i$	$Comp_i$
0	0	0	0	0	0	0	1	0
0	0	1	+A	0	0	1	0	1
0	1	0	+A	0	0	1	0	1
0	1	1	+2A	0	1	0	0	1
1	0	0	-2A	1	1	0	0	1
1	0	1	-A	1	0	1	0	1
1	1	0	-A	1	0	1	0	1
1	1	1	0	1	0	0	1	0

The proposed Booth encoder structure is shown in figure 4. It has an improvement in its design from the previous encoders that since the proposed encoder is used for fixed width modified Booth multiplication, the Cor_i bits are not generated and used for partial product generation. This is because of the fact that in the proposed design, neither the LP_{minor} partial product bits nor the Cor_i bits are taken by the compensation circuit for producing the necessary compensation.

The partial product array for the proposed architecture is shoen in figure. A compensation value '*ecomp*' is added as the approximate carry to the LP_{major} such that it is been added with the retained adder cells and effective compensation is made possible. The sign extension scheme used here is the sign generate sign extension scheme.

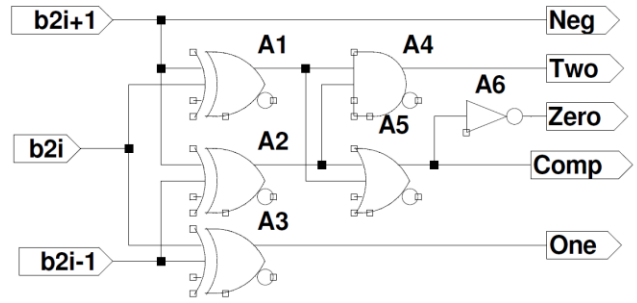

Fig. 4. Proposed modified Booth encoder.

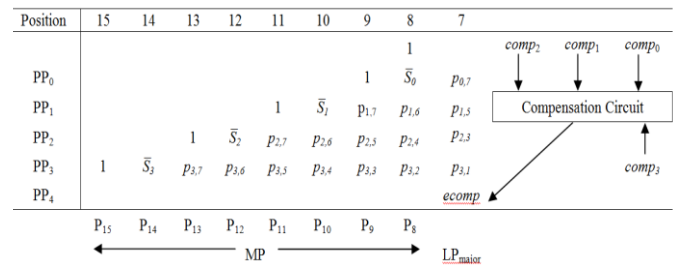

Fig.5. Partial product matrix for proposed *n* bit fixed width modified Booth multiplier

3.2 Compensation Circuit

The compensation circuit proposed here is based on majority selection logic such that there will be a carry for any of two rows of the partial product being not completely zero. The PP_3 and PP_4 rows need not be taken into consideration since there are no partial products in these rows which are to be considered. The design of the proposed compensation circuit can be got from the truth table given by table III.

Table III. Truth table for compensation circuit.

Comp3	Comp2	Comp1	Comp0	ecomp
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Karnaugh map reductions are made for the truth table. The equation using Karnaugh map reduction can be given as:

$$ecomp = (Comp_3 \,.\, Comp_2 \,.\, Comp_0) + (Comp_3 \,.\, Comp_2 \,.\, Comp_1) + (Comp_2 \,.\, Comp_1 \,.\, Comp_0) + (Comp_3 \,.\, Comp_1 \,.\, Comp_0) \quad (5)$$

The circuit implementation for the equation is shown in figure 6.

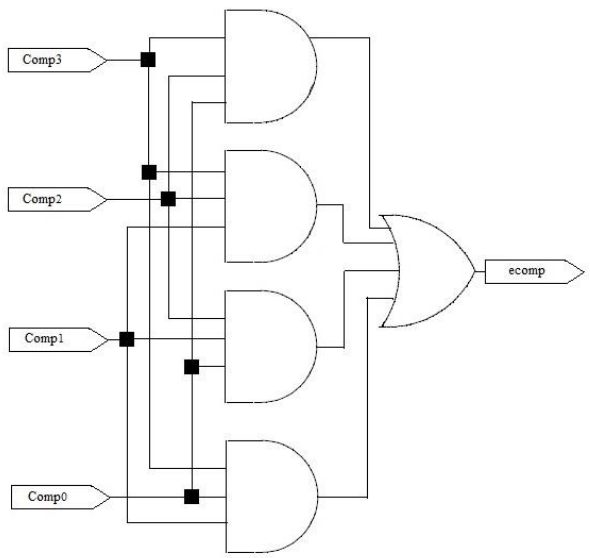

Fig. 6. Proposed compensation circuit.

3.3 Adder Arrray

The summand summation unit is processed using the carry saved adder (CSA) tree and the carry propogate adder (CPA). Figure 7. shows adder array for the proposed fixed width modified Booth multiplier. The summand matrix needs three CSA tree levels. Although the compensation vector must be applied to partial product row PP_4, through careful arrangement the CSA tree level does not increase.

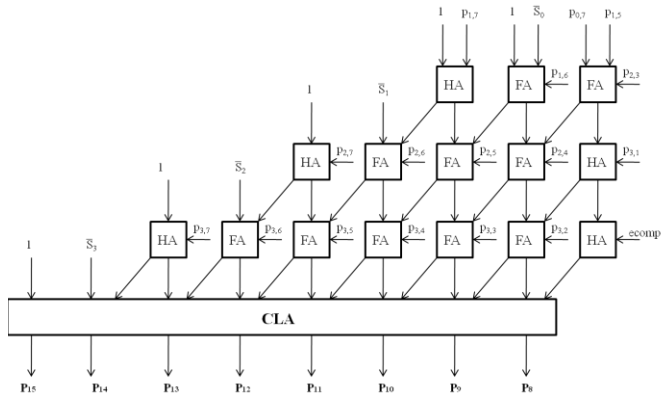

Fig. 7. Adder array for the proposed fixed width Booth multiplier.

4 Experimental Results

To compare the characteristics of fixed width modified Booth multipliers, the proposed circuit as well as the SC fixed width modified Booth multipliers was implemented in Verilog HDL. These fixed-width Booth multipliers were synthesized through utilizing Leonardo Spectrum LS2009a and Xilinx ISE 8.1. The implementation results including number of gates and critical path delay are compared. The simulation result is shown in figure 8.

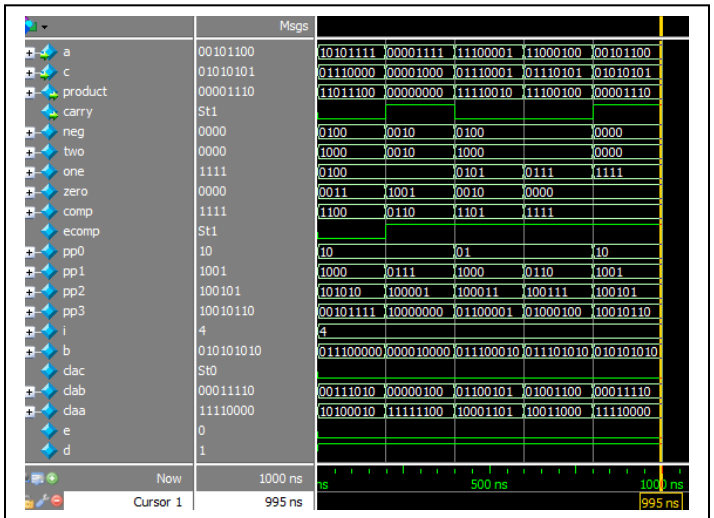

Fig. 8. Simulation result

Table IV. Synthesis report

	Delay	Number of gates
FWMBM in reference[1]	25.651ns	234
Proposed FWMBM	22.428ns	223

The proposed fixed width modified Booth multiplier can be considered to be showing better results.

5 Conclusion

Through this project, a high-accuracy fixed-width modified Booth multiplier has been proposed. In the proposed multiplier, the partial product matrix of Booth multiplication was modified such that the adder cells needed for the computation of the n least significant output bits of the multiplier are removed hence making significant hardware complexity reduction and power saving.

The Booth encoder structure particularly or fixed width multiplication is designed. In addition, a simplified compensation network using simple logic gates has been designed to realize the compensation function. Implementation results showed that the proposed fixed-width modified Booth multiplier can achieve reduction in the area as well as critical path delay when compared with the previous circuit using SC compensation.

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